PATENT

UNITED STATES PATENT AND TRADEMARK OFFICE
Honeywell Case No. H0004446-1600
(MBHB Case No. 02-1202)

In the Application of:	)	
	)	
Roy M. Carlson and David O. Erstad	)	Art Unit: TBA
	)	
Serial No.: TBA	)	
	)	Examiner: TBA
Filed: December 9, 2003	)	
	)	
For: System Level Hardening of Null Convention Logic Circuits	)	

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the duty of disclosure provided by 35 C.F.R. § 1.56 and §§ 1.97-98, the Applicants wish to make the following references of record in the above-identified application. Copies of the non-patent references are enclosed. The references are also listed in the PTO-1449 form enclosed herewith. It is requested that the documents be given careful consideration and that they be cited of record in the prosecution history of the present application so that they will appear on the face of the patent issuing from the present application.

Portions of the references may be material to the examination of the pending claims, however no such admission is intended. 37 C.F.R. 1.97 (h). The references have not been reviewed in sufficient detail to make any other representation and, in particular, no

FORM PTO-1449 (Rev. 2-32)	U. S. Department of Commerce Patent and Trademark Office	Atty. Docket No. H0004446-1600	Serial No. TBA
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several Sheets is Necessary)		Applicant: Roy M. Carlson and David O. Erstad	
		Filing Date: December 9, 2003	Group: TBA

U. S. PUBLISHED PATENT APPLICATION DOCUMENTS

Examiner Initials	No.	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	1.	2003/0091038 A1	05/15/03	Hagedorn	370	359	11/09/01

U. S. PATENT DOCUMENTS

Examiner Initials	No.	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	2.	4,782,467	11/01/88	Belt et al.	365	154	09/25/87
	3.	4,805,148	02/14/89	Diehl-Nagle et al.	365	154	11/22/85
	4.	5,305,463	04/19/94	Fant et al.	395	800	06/08/93
	5.	5,406,513	04/11/95	Canaris et al.	365	181	02/05/93
	6.	5,640,105	06/17/97	Sobelman et al.	326	36	09/10/96
	7.	5,652,902	07/29/97	Fant	395	800	10/05/94
	8.	5,656,948	08/12/97	Sobelman et al.	326	35	09/09/96
	9.	5,664,211	09/02/97	Sobelman et al.	395	141	10/05/94

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Examiner Initials	No.	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	10.	5,664,212	09/02/97	Fant et al.	395	141	03/31/94
	11.	5,764,081	06/09/98	Fant et al.	326	63	01/22/97
	12.	5,796,962	08/18/98	Fant et al.	395	306	04/18/95
	13.	5,793,662	08/11/98	Duncan et al.	364	768	06/07/95
	14.	5,828,228	10/27/98	Fant et al.	326	35	09/02/97
	15.	5,896,541	04/20/99	Fant et al.	395	800.18	06/02/95
	16.	5,907,693	05/25/99	Fant et al.	395	384	09/24/97
	17.	5,930,522	07/27/99	Fant	395	800.25	06/07/95
	18.	5,977,663	11/02/99	Fant et al.	307	251	09/24/97
	19.	5,986,466	11/16/99	Sobelman et al.	326	39	10/08/97
	20.	6,020,754	02/01/00	Sobelman et al.	326	35	03/31/98
	21.	6,031,390	02/29/00	Fant et al.	326	36	12/16/97
	22.	6,043,674	03/28/00	Sobelman	326	35	01/08/98
	23.	6,052,770	04/18/00	Fant	712	14	07/28/97
	24.	6,128,678	10/03/00	Masteller	710	52	08/28/98
	25.	6,262,593	07/17/01	Sobelman et al.	326	35	01/08/98
	26.	6,278,287	08/21/01	Baze	326	9	10/27/99
	27.	6,292,128	09/18/01	Tsui et al.	342	13	04/04/00
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	29.	6,313,660	11/06/01	Sobelman et al.	326	39	10/18/99
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Examiner Initials	No.	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	33.	6,526,542	02/25/03	Kondratyev	716	2	05/07/01

FOREIGN PATENT DOCUMENTS

Examiner Initials	No.	Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc).

Examiner Initials	No.	Document
	34.	Maher, Michael, "Radiation Design Considerations Using CMOS Logic," National Semiconductor Application Note 926, January 1994
	35.	"Throw Away the Clock," Theseus Logic – Benefits of NCL – EMI, http://www.theseus.com/_AboutNCL.htm, printed November 19, 2002
	36.	Sobelman, Gerald E. and Karl Fant, "CMOS Circuit Design of Threshold Gates with Hysteresis," Pages 1 - 5
	37.	Fant, Karl M. and Scott A. Brandt, "NULL Convention Logic," Theseus Logic: Setting the Standard for Clockless Systems, 1997

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformation and not considered. Include copy of this form with next communication.

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representation is intended as to the relative importance of any portion of the references. This Statement is not a representation that the cited references have effective dates early enough to be "prior art" within the meaning of 35 U.S.C. sections 102 or 103, nor is this submission to be construed as a representation that a search has been made.

CITED REFERENCES

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36.	Sobelman, Gerald E. and Karl Fant, "CMOS Circuit Design of Threshold Gates with Hysteresis," Pages 1 - 5
37.	Fant, Karl M. and Scott A. Brandt, "NULL Convention Logic," Theseus Logic: Setting th Standard for Clockless Systems, 1997

Respectfully submitted,

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Date: December 9, 2003

By: 

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